REMARKS

These remarks follow the order of the paragraphs of the office action. Relevant portions of the office action are shown indented and italicized.

Applicants express their appreciation for the opportunity to discuss the application and rejections with the Examiner. It is unfortunate that agreement was not reached. Amendments are made in an attempt to satisfy the Examiner's comments.

DETAILED ACTION
Claim Rejections -35 USC § 112

1. The following is a quotation of the first paragraph of 36 USC 112: The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, dear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 1-10, 17-18, 21-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites a buffer storing indications of interrupts in line 2, "moving the contents of the buffer to the payload portion of the control data block, and sending the control data block to the host computer system' in lines 7-9. The recitations suggest that indications of interrupts are being transferred to the host computer system, yet claim 1 also recites "said apparatus for transferring interrupts from the peripheral device to a host computer in lines 3-4. The specification does not disclose transferring interrupts and indications of interrupts to the host computer.

In response, the applicants respectfully states that claims are amended based on the discussion with the Examiner to better express the invention claimed. Examiner requested backup in the

specification for the elements of the claims. The following includes some of the references in the application to an indication. Applicants are using the word interrupt to be any indication. However, to overcome the rejection, the word indication event' is used in claim 1.

In the specification, events include at least of: internal flag, a status indication of completion of the read operation, an indication that a new header is waiting in the HeaderIn FIFO , or an indication that a packet header is ready for the RX HeaderIn FIFO 640, an indication is sent to the RX processor 160. Also, see:

> p 23, line 2: At the end of the header processing, a descriptor, or a set of descriptors, are written to the LCP RX HeaderOut FIFO 410, and an indication is triggered

> pg. 29, line 1: For example, in the case of a reliable transmission, the TX processor 150. Reads internal registers indicating the status of a packet transmission. In the case of reliable reception, the RX processor 160 gets a completion indication as a received packet which includes an acknowledgment. In the case of a receive DMA completion, the RX processor 160 uses frame completion information. In the case of a transmit DMA completion, the TX processor 150 indicates the reception of a frame for transmission in the adapter 80. A completion queue can be used by a single TX or RX LCP channel or may shared by multiple channels. Micro code in the adapter 80 updates a status queue by initiating a frame descriptor into a command queue of the RX LCP engine 360. Referring to Figure 11, the status is transferred to the memory 60 of the host 10 via a completion status LCP 900 comprising a completion queue 920. The completion queue 900 is continuous (either physically or virtually) and is located in the memory 60 of the host 10. For example, the completion queue can be held in a continuous buffer. Entries 930 in the completion queue preferably have a fixed size. Each entry holds a pointer 940 to the head of a buffer 950 associated with a receive LCP 910. The buffer 950 is filled by the packet 960 associated with the completion status..

> page 38, line 21:

At step 1640, once processing of the descriptor is completed, a completion event indication 1650 is sent to an interrupt FIFO buffer 1660 in the ISOC 120 by an interrupt controller of the ISOC 120.

page 39, line 10: The operation of the ISOC 120 following a completion event varies depending on the value of the EventMask and the CompletionEvent bit in the context 140. If the EventMask bit is cleared, an indication is sent to the interrupt controller of the ISOC 120 and the EventMask bit is set by the ISOC 120.

pg 39, line 20: The operation of the ISOC 120 following a completion event varies depending on the value of the EventMask and the CompletionEvent bit in the context 140. If the EventMask bit is cleared, an indication is sent to the interrupt controller of the ISOC 120 and the EventMask bit is set by the ISOC 120.

p40, l 11: There is at least a predetermined minimum number of event completion indications in the FIFO 1660 and a predetermined minimum time period has passed;

3. Claims 11-16 19-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject mailer, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which t is most nearly connected, to make and/or use the invention.

It appears that there is no support for moving the contents of the buffer to the corresponding fields of the payload portion" - as page 38, lines 25-26 merely discloses "when preset conditions are met, an Interrupt Control Block (ICB) 1680 is generated by the ISOC 120 from the information stored in the interrupt FIFO 1660".

In response, the applicants respectfully states that... ... .

4. Claims 13-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In response, the applicants respectfully states that... ... .

Claim 13 recites "at least a predetermined plurality of indications is stored in the buffer". Claim 14 recites at least one indication is stored in the buffer".

In response, the applicants respectfully states that... ... .

Claim 15 recites "a count indicative of the number of indications included in the payload portion".
The claims suggest that interrupts and indications are two different entities, while the specification only discloses only one entity being stored in the buffer and the count being indicative of only one entity.

In response, the applicants respectfully states that... ... .

5. Claims 10, 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The examiner cannot find support for the limitations of the claims. In particular, it is not clear what constitute the claimed apparatus, the claimed host processing system, the claimed memory of the host processing system, the claimed data processing system, the claimed host computer, and the claimed memory of the host computer system. Applicant is required to specifically point out where to find the support for the limitations of the claims in the specification, by page and line number - and in particular, applicant is required to map out each of the elements claimed with the teachings of the specification.

In response, the applicants respectfully states that... ... .

6. No art rejection was made to claims 1-16, 21-22 because the scope of the claims is ambiguous, and it is not possible for the examiner to apply prior art without making a great deal of speculation.

In response, the applicants respectfully states that... ... .

Claim Rejections -35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printers publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated Raasch et al. (US 5,333,273).

In response, the applicant respectfully states that Claims 17-20 are not made patentable by the invention of Raasch. The present invention, claimed in Claims 17-20, provides:

> "Methods, systems and apparatus for transferring interrupts from a peripheral device to a host computer system is described. In an example embodiment, an apparatus comprises a buffer for storing indications of interrupts generated by the peripheral device. In response to a preset condition being met, a controller generates a control data block having a payload portion, moves the contents of the buffer to the payload portion of the control data block, and sends the control data block to the host computer system."

Whereas, the cited art to Raasch, US Patent 5,333,273, filed: September 3, 1992, is entitled: "Protected hot key function for microprocessor-based computer system". The abstract reads: "An ISA-compatible computer system includes an additional function key on its keyboard. The additional function key does not have a defined function for conventional ISA-standard computers. When a conventional alphanumeric key or function key is activated on the keyboard, the computer system is interrupted using IRQ1 and the key information is communicated to the computer system so that the computer system can respond in a conventional manner using a conventional keyboard interrupt handling routine. When the additional function key and an alphanumeric key are activated in combination, a second interrupt different from the IRQ1 interrupt is activated (e.g., IRQ15). The computer system responds to the second interrupt by inputting an identification of the activated alphanumeric key and performing a selected predetermined function in response thereto. The handling of the second interrupt is performed by a separate interrupt handling routine within the computer system so that conventional terminate and stay resident (TSR) programs that intercept conventional keyboard inputs cannot readily

intercept keyboard input initiated by the additional function key ". Thus Raasch is not concerned with or teach. indications of events or a preset condition as in the claims. Thus, all claims are allowable.

9. As per claims 17, 19, Raasch teaches a computer program product (or article of manufacture) comprising a computer usable medium [138, FIG. 1] having computer readable program code means [BIOS: col. 5, lines 18-21] embodied therein for causing transfer of interrupts [col. 4, lines 66-68], the computer readable program code means in said computer program product (or article of manufacture) comprising computer readable program code means [BIOS: col. 5, lines 18-21] for causing a computer (100, FIG. 1] to effect the functions of the apparatus of claim 1 (or the method of claim 11)- as the BIOS would cause a computer to effect the functions of any apparatus, hence including functions of the apparatus of claim 1; and as the BIOS would cause a computer to effect the steps of any method, hence including the steps of the method of claim 11.

In response, the applicants respectfully states that Raasch is not concerned with or teach. indications of events or a preset condition as in the claims. Thus, all claims are allowable.

10. As per claim 18, Raasch teaches a computer program product comprising a computer usable medium [138. FIG. 11 having computer readable program code means [BIOS: col. 5, lines 18-21] embodied therein for causing data processing [col. 5, lines 18-21], the computer readable program code means in said computer program product comprising computer readable program code means [BIOS: col. 5, lines 18-21] for causing a computer [100, FIG. 1] to effect the functions of the apparatus of claim 10- as the BIOS would cause the computer to effect the functions of any apparatus, hence including the functions of the apparatus of claim 10.

In response, the applicants respectfully states that Raasch is not concerned with or teach. indications of events or a preset condition as in the claims. Thus, all claims are allowable.

11. As per claim 20, Raasch teaches a program storage device [138, FIG. 1] readable by machine [100, FIG. 1], tangibly embodying a program of instructions (BIOS: col. 5, lines 18-21] executable by the machine to perform method steps for transferring interrupts [col. 4, lines 66-68], said method steps comprising the steps of claim 11 (the BIOS would cause a computer to effect the steps of any method, hence including the steps of the method of claim 11).

In response, the applicants respectfully states that Raasch is not concerned with or teach. indications of events or a preset condition as in the claims. Thus, all claims are allowable.

It is anticipated that this amendment brings all claims to allowance.

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